Tikrit university

Collage of Engineering Shirqat

Department of Electrical Engineering

Second Class

Electronic I

Chapter 4
DC Biasing—BJTs

Prepared by

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4.1 INTRODUCTION

The analysis or design of a transistor amplifier requires a knowledge of both the dc and the ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality,

any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.

The analysis or design of any electronic amplifier therefore has two components: a dc and an ac portion. Fortunately, the superposition theorem is applicable, and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa. the following important basic relationships for a transistor:

$$V_{BE} \cong 0.7\ \text{V} \tag{4.1}$$

$$I_E = (\beta + 1)I_B \cong I_C \tag{4.2}$$

$$I_C = \beta I_B \tag{4.3}$$

4.2 OPERATING POINT

Figure 4.1 shows a general output device characteristic with operating points indicated

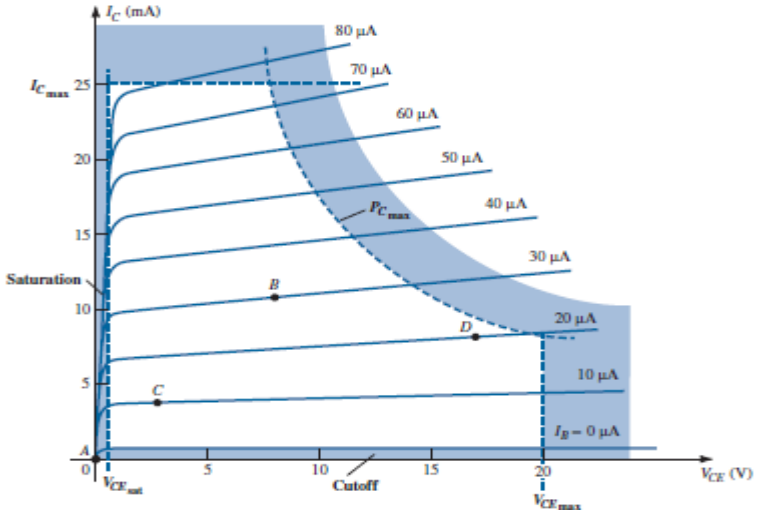

Fig 4.1 Various operating points within the limits of operation of a transistor

For the BJT to be biased in its linear or active operating region the following must be true:

1. The base–emitter junction must be forward-biased (p-region voltage more positive), with a resulting forward-bias voltage of about 0.6 V to 0.7 V.

2. The base–collector junction must be reverse-biased (n-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided

as follows:

1. Linear-region operation:

Base–emitter junction forward-biased

Base–collector junction reverse-biased

2. *Cutoff-region operation:*

Base–emitter junction reverse-biased

Base–collector junction reverse-biased

3. *Saturation-region operation:*

Base–emitter junction forward-biased

Base–collector junction forward-biased

4.3 FIXED-BIAS CONFIGURATION

The fixed-bias circuit of Fig. 4.2 is the simplest transistor dc bias configuration. Even though the network employs a npn transistor, the equations and calculations apply equally well to a pnp transistor configuration merely by changing all current directions and voltage polarities. The current directions of Fig. 4.2 are the actual current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent because the reactance of a capacitor is a function of the applied frequency. For dc, f = 0 Hz, and $X_C = 1/2\pi fC = 1/2\pi(0)C = \infty$.

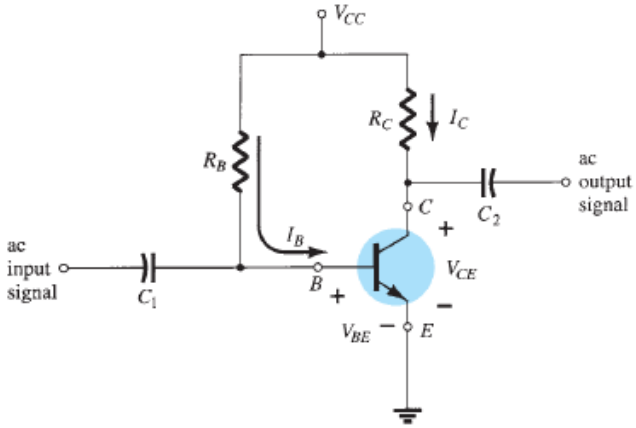

FIG. 4.2
Fixed-bias circuit.

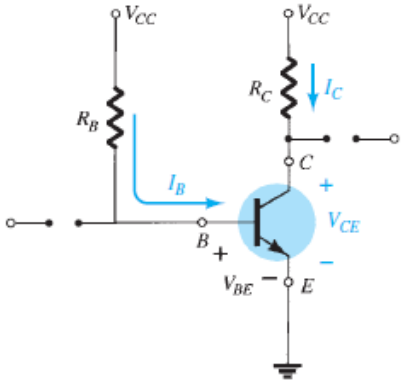

FIG. 4.3
DC equivalent of Fig. 4.2.

Forward Bias of Base–Emitter

Consider first the base–emitter circuit loop of Fig. 4.4 . Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

+VCC - IBRB - VBE = 0

Note the polarity of the voltage drop across RB as established by the indicated direction of IB. Solving the equation for the current IB results in the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad (4.4)$$

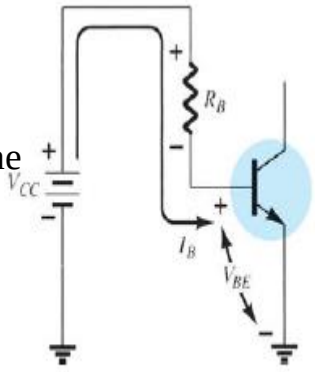

FIG. 4.4
Base–emitter loop.

Collector–Emitter Loop

The collector–emitter section of the network appears in Fig. 4.5 with the indicated direction of current *IC* and the resulting polarity across *RC* . The magnitude of the collector current is related directly to *IB* through $I_C = \beta I_B$

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 results in the following:

VCE + ICRC - VCC = 0

$$V_{CE} = V_{CC} - I_C R_C \qquad (4.6)$$

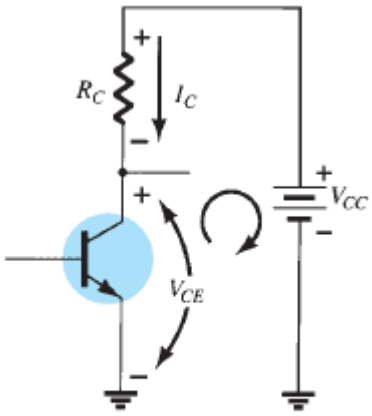

FIG. 4.5
Collector–emitter loop.

$$V_{CE} = V_C - V_E \quad (4.7)$$

where *V CE* is the voltage from collector to emitter and *VC* and *VE* are the voltages from collector and emitter to ground, respectively. *In this case,* since *V E* = 0 V, we have

$V_{CE} = V_C$ (4.8). In addition, because $V_{BE} = V_B - V_E$ (4.9)

and *VE* =0 V, then $V_{BE} = V_B$ **(4.10)**

EXAMPLE 4.1 Determine the following for the fixed-bias configuration of Fig. 4.7.

a. I_{B_Q} and I_{C_Q}.
b. V_{CE_Q}.
c. V_B and V_C.
d. V_{BC}.

Solution:

a. Eq. (4.4): $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

Eq. (4.5): $$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

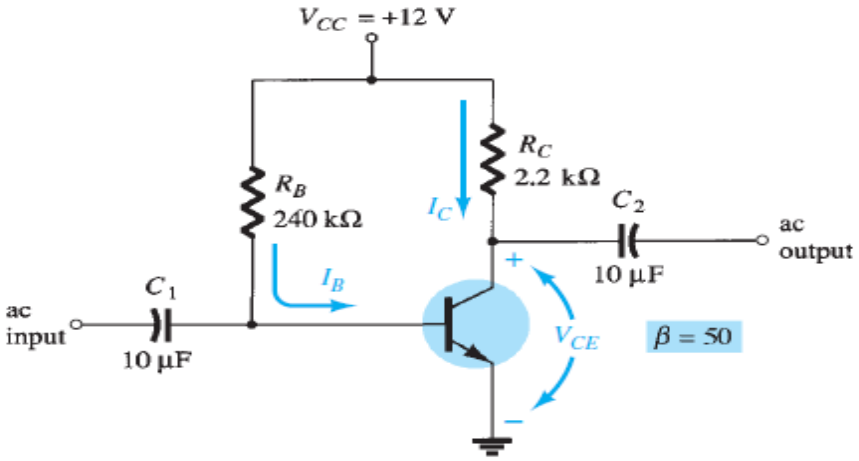

FIG. 4.7
DC fixed-bias circuit for Example 4.1.

b. Eq. (4.6): $$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\ V}$$

c. $V_B = V_{BE} = \mathbf{0.7\ V}$
$V_C = V_{CE} = \mathbf{6.83\ V}$

d. Using double-subscript notation yields
$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$

Transistor Saturation

For a transistor operating in the saturation region, the current is a maximum value for the particular design. the current is relatively high, and the voltage VCE is assumed to be 0 V.

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0\text{ V}}{I_{C_{sat}}} = 0\ \Omega$$

For the fixed-bias configuration of Fig. 4.10, The short circuit has been applied, causing the voltage across R C to be the applied voltage VCC .The resulting saturation current for the fixed-bias configuration is

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} \quad (4.11)$$

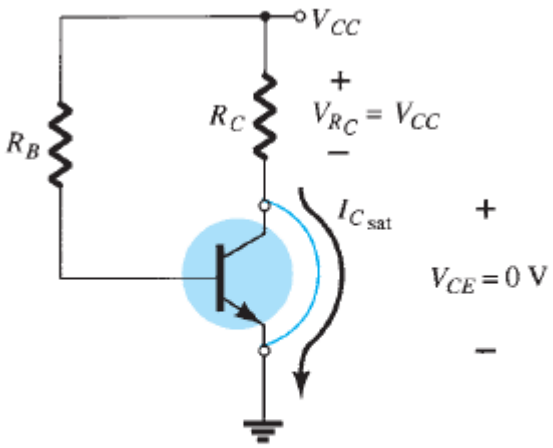

FIG. 4.10
Determining $I_{C_{sat}}$ for the fixed-bias configuration.

Once ICsat is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

EXAMPLE 4.2 Determine the saturation level for the network of Fig. 4.7.

Solution:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{12\text{ V}}{2.2\text{ k}\Omega} = \mathbf{5.45\text{ mA}}$$

Load-Line Analysis

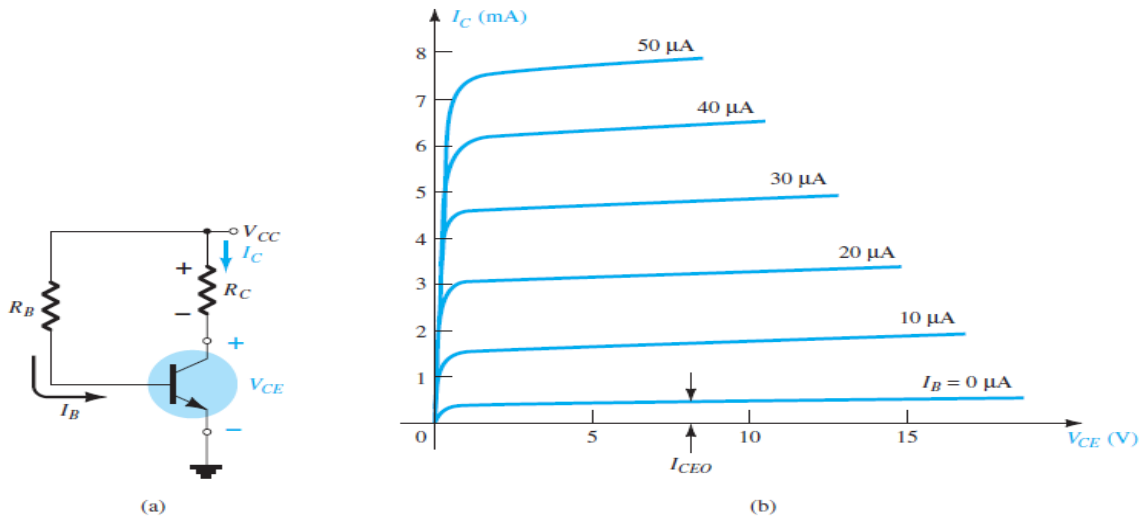

FIG. 4.11
Load-line analysis: (a) the network; (b) the device characteristics.

The network of Fig. 4.11a establishes an output equation that relates the variables I C and V CE in the following manner: $V_{CE} = V_{CC} - I_C R_C$ (4.12)

If we *choose I C* to be 0 mA, we are specifying the horizontal axis as the line on which one point is located. By substituting *I C* _ 0 mA into Eq. (4.12), we find that *VCE* = *VCC* - (0)*RC* $V_{CE} = V_{CC}|_{I_C=0\text{ mA}}$ (4.13) defining one point for the straight line as shown in Fig. 4.12 .

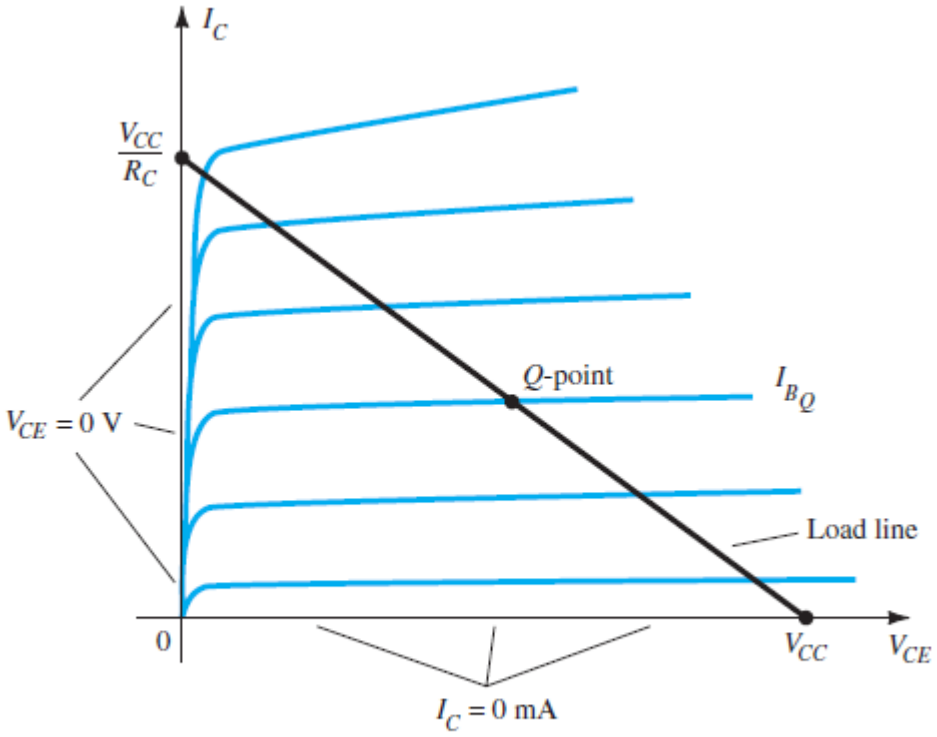

FIG. 4.12
Fixed-bias load line.

If we now choose VCE to be 0 V, which establishes the vertical axis as the line on which the second point will be defined, we find that IC is determined by the following equation: 0 = VCC – ICRC and $I_C = \frac{V_{CC}}{R_C}\Big|_{V_{CE}=0\text{ V}}$ **(4.14)**

EXAMPLE 4.3 Given the load line of Fig. 4.16 and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

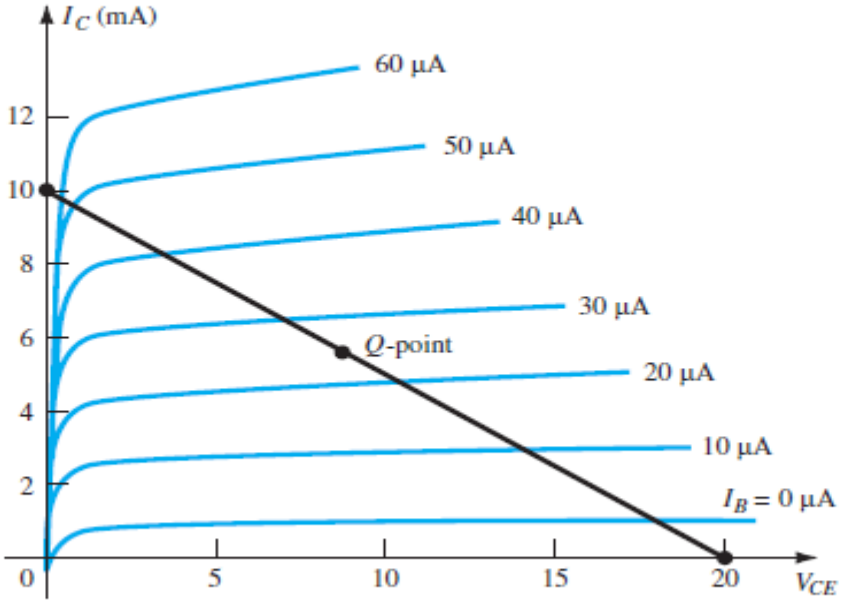

FIG. 4.16
Example 4.3.

Solution: From Fig. 4.16,

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\ \text{mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\ \text{V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{10\ \text{mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\ \text{V} - 0.7\ \text{V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

4.4 EMITTER-BIAS CONFIGURATION

The analysis will be performed by first examining the base–emitter loop and then using the results to investigate the collector–emitter loop.

The dc equivalent of Fig. 4.17 appears in Fig 4.18 with a separation of the source to create an input and output section.

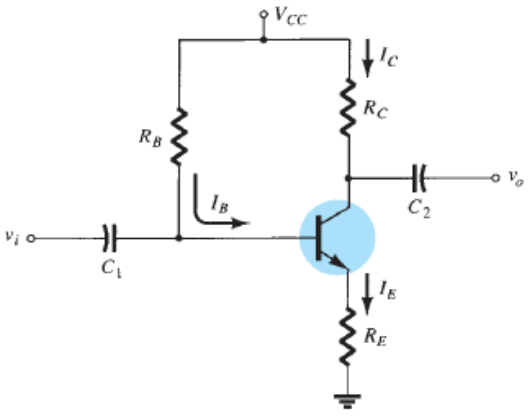

FIG. 4.17 *BJT bias circuit with emitter resistor*

Base–Emitter Loop

The base–emitter loop of the network of Fig. 4.18 can be redrawn as shown in Fig. 4.19 .

+VCC - IBRB - VBE - IERE = 0 **(4.15)**

IE = (β + 1) IB **(4.16)**

Substituting for I E in Eq. (4.15) results in

VCC - IBRB - VBE - (β + I) IBRE = 0

Grouping terms then provides the following:

-IB(RB + (β + 1)RE) + VCC - VBE = 0

Multiplying through by (-1),

we have IB(RB + (β + 1)RE) - VCC + VBE = 0

with IB(RB + (β + 1)RE) = VCC – VBE

and solving for *I B* gives $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ **(4.17)**

Such is the case for the network of Fig. 4.20 . Solving for the current *IB* results in the same equation as obtained above

Note that aside from the base-to-emitter voltage VBE, the resistor RE is reflected back to the input base circuit by a factor (β + 1). In other words, the emitter resistor, which is part of the collector–emitter loop, "appears as" (β +1) RE in the base–emitter loop. Because b is typically 50 or more, the emitter resistor appears to be a great deal larger in the base circuit. In general, therefore, for the configuration *of Fig. 4.21* ,

$$R_i = (\beta + 1)R_E \quad \textbf{(4.18)}$$

Collector–Emitter Loop

The collector–emitter loop appears in Fig. 4.22 . Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction results in

+IERE + VCE + ICRC - VCC = 0

Substituting IE = IC and grouping terms gives

VCE - VCC + IC (RC + RE) = 0

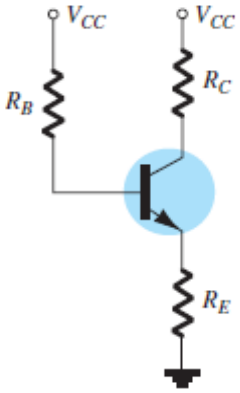

FIG. 4.18
DC equivalent of Fig. 4.17.

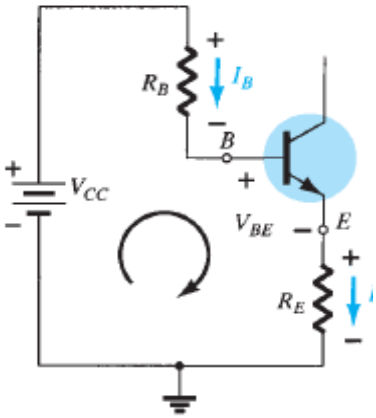

FIG. 4.19
Base–emitter loop.

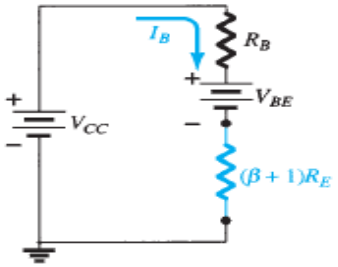

FIG. 4.20
Network derived from Eq. (4.17).

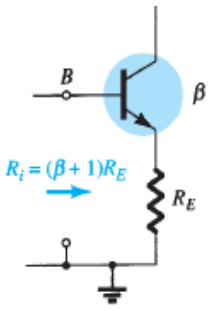

FIG. 4.21
Reflected impedance level of R_E.

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad (19)$$

$$V_E = I_E R_E \quad (20)$$

whereas the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$V_C = V_{CE} + V_E \quad (21)$$

or

$$V_C = V_{CC} - I_C R_C \quad (22)$$

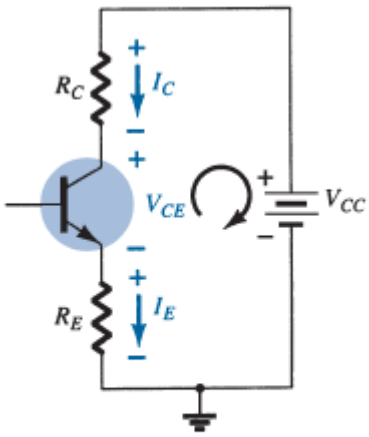

FIG. 22
Collector–emitter loop.

The voltage at the base with respect to ground can be determined using Fig. 18

$$V_B = V_{CC} - I_B R_B \quad (23)$$

or

$$V_B = V_{BE} + V_E \quad (24)$$

EXAMPLE 4 For the emitter-bias network of Fig. 23, determine:

a. I_B.
b. I_C.
c. V_{CE}.
d. V_C.
e. V_E.
f. V_B.
g. V_{BC}.

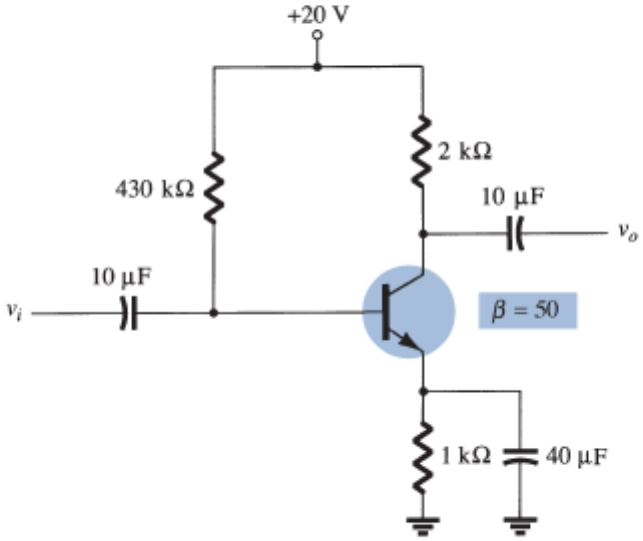

FIG. 23
Emitter-stabilized bias circuit for Example 4.

Solution:

a. Eq. (17): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

b. $$I_C = \beta I_B$$
$$= (50)(40.1\ \mu\text{A})$$
$$\cong \mathbf{2.01\ mA}$$

c. Eq. (19): $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$$
$$= \mathbf{13.97\ V}$$

d. $$V_C = V_{CC} - I_C R_C$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$$
$$= \mathbf{15.98\ V}$$

e. $$V_E = V_C - V_{CE}$$
$$= 15.98\text{ V} - 13.97\text{ V}$$
$$= \mathbf{2.01\ V}$$

or $$V_E = I_E R_E \cong I_C R_E$$
$$= (2.01\text{ mA})(1\text{ k}\Omega)$$
$$= \mathbf{2.01\ V}$$

f. $$V_B = V_{BE} + V_E$$
$$= 0.7\text{ V} + 2.01\text{ V}$$
$$= \mathbf{2.71\ V}$$

g. $$V_{BC} = V_B - V_C$$
$$= 2.71\text{ V} - 15.98\text{ V}$$
$$= \mathbf{-13.27\ V}\ \text{(reverse-biased as required)}$$

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 24 and calculate the resulting collector current. For Fig. 24

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} \qquad (25)$$

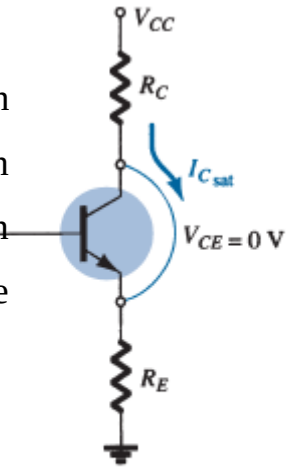

FIG. 24
Determining $I_{C_{sat}}$ for the emitter-stabilized bias circuit.

EXAMPLE 6 Determine the saturation current for the network of Example 4.

Solution:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$
$$= \frac{20\text{ V}}{2\text{ k}\Omega + 1\text{ k}\Omega} = \frac{20\text{ V}}{3\text{ k}\Omega}$$
$$= \mathbf{6.67\text{ mA}}$$

which is about three times the level of I_{C_Q} for Example 4.

Load-Line analysis

The collector–emitter loop equation that defines the load line is $VCE = VCC - IC(RC + RE)$

Choosing $IC = 0$ mA gives

$$V_{CE} = V_{CC}\big|_{I_C=0\text{ mA}} \qquad (26)$$

as obtained for the fixed-bias configuration. Choosing $VCE = 0$ V gives

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE}=0\text{ V}} \qquad (27)$$

as shown in Fig. 25. Different levels of IBQ will, of course, move the Q-point up or down the load line.

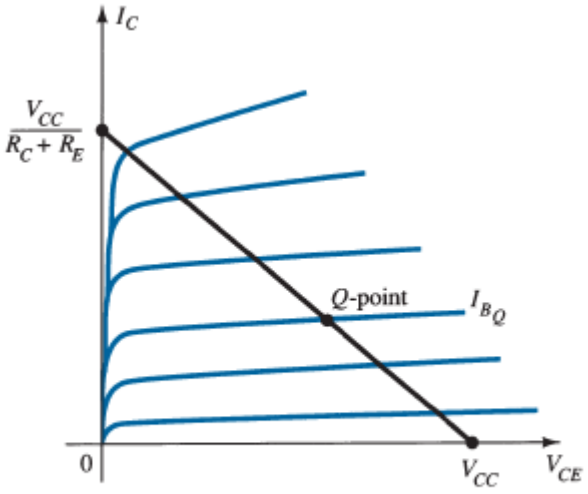

FIG. 25
Load line for the emitter-bias configuration.

EXAMPLE 7

a. Draw the load line for the network of Fig. 26a on the characteristics for the transistor appearing in Fig. 26b.
b. For a Q-point at the intersection of the load line with a base current of 15 μA, find the values of I_{C_Q} and V_{CE_Q}.
c. Determine the dc beta at the Q-point.
d. Using the beta for the network determined in part c, calculate the required value of R_B and suggest a possible standard value.

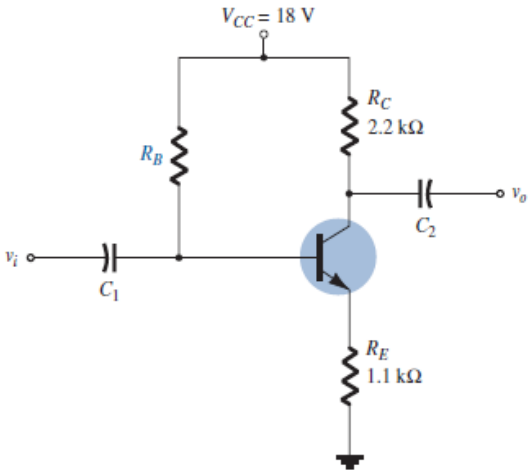

FIG. 26a
Network for Example 7.

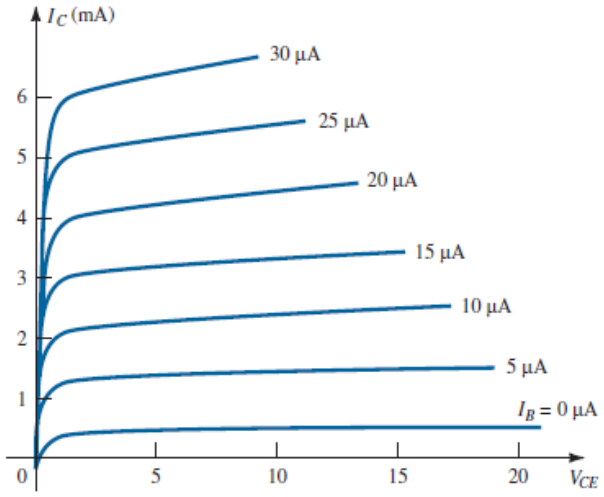

FIG. 26b
Example 7.

Solution:

a. Two points on the characteristics are required to draw the load line.

At $V_{CE} = 0$ V: $I_C = \dfrac{V_{CC}}{R_C + R_E} = \dfrac{18\text{ V}}{2.2\text{ k}\Omega + 1.1\text{ k}\Omega} = \dfrac{18\text{ V}}{3.3\text{ k}\Omega} = 5.45\text{ mA}$

At $I_C = 0$ mA: $V_{CE} = V_{CC} = 18$ V

The resulting load line appears in Fig. 27.

b. From the characteristics of Fig. 27 we find

$V_{CE_Q} \cong$ **7.5 V**, $I_{C_Q} \cong$ **3.3 mA**

c. The resulting dc beta is:

$$\beta = \frac{I_{C_Q}}{I_{B_Q}} = \frac{3.3\text{ mA}}{15\ \mu\text{A}} = \mathbf{220}$$

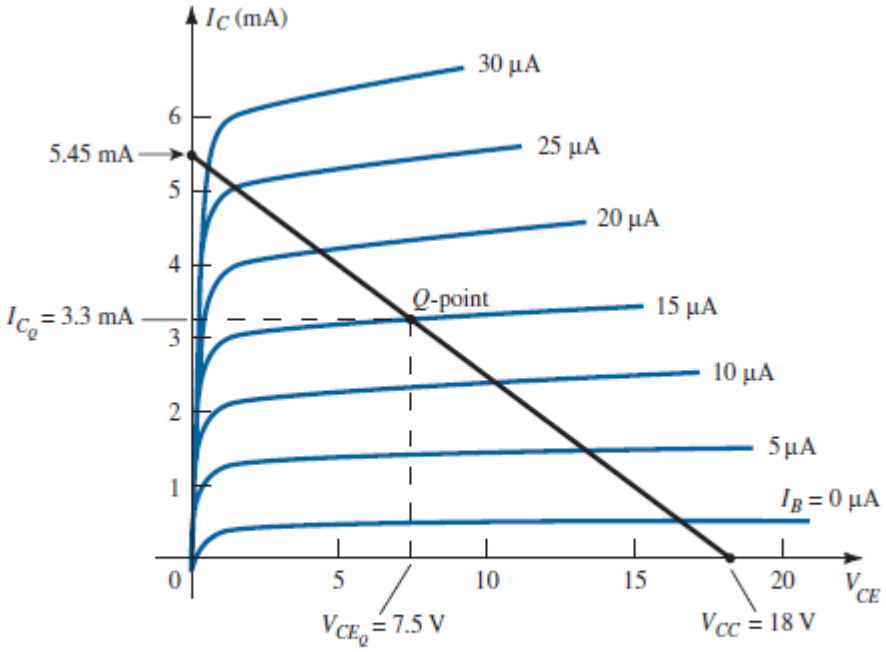

FIG. 27
Example 7.

d. Applying Eq. 17:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{18\text{ V} - 0.7\text{ V}}{R_B + (220 + 1)(1.1\text{ k}\Omega)}$$

$$\text{and } 15\ \mu\text{A} = \frac{17.3\text{ V}}{R_B + (221)(1.1\text{ k}\Omega)} = \frac{17.3\text{ V}}{R_B + 243.1\text{ k}\Omega}$$

so that $(15\ \mu\text{A})(R_B) + (15\ \mu\text{A})(243.1\text{ k}\Omega) = 17.3\text{ V}$

and $(15\ \mu\text{A})(R_B) = 17.3\text{ V} - 3.65\text{ V} = 13.65\text{ V}$

resulting in $R_B + \frac{13.65\text{ V}}{15\ \mu\text{A}} = \mathbf{910\text{ k}\Omega}$